10/604,962

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Allen et al.

Serial No.: 10/604,962 Group Art Unit: 2822

Filed: 08/28/03 Examiner: Siek, Vuthe

For: THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE YIELD AND RELIABLITY OF VLSI DESIGNS

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action mailed March 8, 2005, please amend the above-identified patent application as follows:

IN THE ABSTRACT

Please replace the Abstract as follows:

Certificate of Transmission by Facsimile

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (Fax No. 703-872-9313) on 4/6/05

Frederick W. Gibb, III

ABSTRACT

The invention provides a method and structure for optimizing placement of redundant vias within an integrated circuit design. The invention first locates target vias by determining which vias do not have a redundant via. Then, the invention draws marker shapes on or adjacent to the target vias. The marker shapes are only drawn in a horizontal or vertical direction from each of the target vias. The invention simultaneously expands all of the marker shapes in the first direction to a predetermined length or until the marker shapes reach the limits of a ground rule. During the expanding, different marker shapes will be expanded to different lengths. The invention determines which of the marker shapes were expanded sufficiently to form a valid redundant via to produce a first set of potential redundant vias and the invention eliminates marker shapes that could not be expanded sufficiently to form a valid redundant via.

IN THE CLAIMS:

Please amend the claims as follows:

10/604,962

1. (Original) A method for optimizing placement of redundant vias within an integrated circuit design, said method comprising:

a) locating target vias;

b) drawing marker shapes adjacent to said target vias in a first direction;

c) using an optimizer to simultaneously expand all of said marker shapes either in said first direction, wherein during said expanding, different marker shapes will be expanded to different lengths;

d) determining which of said marker shapes were expanded sufficiently to form a valid redundant via to produce a first set of potential redundant vias;

e) eliminating marker shapes that could not be expanded sufficiently to form a valid redundant via; and

f) repeating steps b-e in a second direction perpendicular to said first direction to produce a second set of potential redundant vias.

2. (Original)The method in claim 1, wherein said locating of said target vias and said drawing of said marker shapes is performed using a shapes-processing program.

3. (Original)The method in claim 1, wherein said expanding of said marker shapes is performed using a minimum perturbation layout-migration tool based on augmented ground rules.

4. (Original)The method in claim 3, wherein said augmented ground rules direct said layout-migration tool how to modify said marker shapes to reveal when space is available to continue said expanding of said marker shapes.

5. (Original)The method in claim 1, wherein said determining which of said marker shapes were expanded sufficiently is performed using a shapes-processing program.

6. (Original)The method in claim 1, wherein said integrated circuit design complies with design ground rules prior to step a.

7. (Original)The method in claim 1, further comprising after step f, adding redundant vias to said integrated circuit design according to output produced by said optimizer.

8. (Original)A method for optimizing placement of redundant vias within an integrated circuit design, said method comprising:

a) locating target vias by determining which vias do not have a redundant via;

b) drawing marker shapes adjacent said target vias, wherein said marker shapes are drawn in a first direction;

c) using an optimizer to simultaneously expand all of said marker shapes in said first direction for a predetermined length or until said marker shapes reach the limits of a ground rule, wherein during said expanding, different marker shapes will be expanded to different lengths;

d) determining which of said marker shapes were expanded sufficiently to form a valid redundant via to produce a first set of potential redundant vias;

e) eliminating marker shapes that could not be expanded sufficiently to form a valid redundant via; and

f) repeating steps b-e in a second direction perpendicular to said first direction to produce a second set of potential redundant vias.

9. (Original)The method in claim 8, wherein said locating of said target vias and said drawing of said marker shapes is performed using a shapes-processing program.

10. (Original)The method in claim 8, wherein said expanding of said marker shapes is performed using a minimum perturbation layout-migration tool based on augmented ground

rules.

11. (Original)The method in claim 10, wherein said augmented ground rules direct said layout-migration tool how to modify said marker shapes to reveal when space is available to continue said expanding of said marker shapes.

12. (Original)The method in claim 8, wherein said determining which of said marker shapes were expanded sufficiently is performed using a shapes-processing program.

13. (Original)The method in claim 8, wherein said integrated circuit design complies with design ground rules prior to step a.

14. (Original)The method in claim 8, further comprising after step f, adding redundant vias to said integrated circuit design according to output produced by said optimizer.

15. (Original)A method for optimizing replacement of stacked vias within an integrated circuit design, said method comprising:

a) locating stacked vias by determining which vias are positioned above or below vias in adjacent wiring levels of said integrated circuit design;

b) drawing marker shapes on or adjacent to said stacked vias in a first direction;

c) using an optimizer to simultaneously expand all of said marker shapes in said first direction for a predetermined length or until said marker shapes reach the limits of a ground rule, wherein during said expanding, different marker shapes will be expanded to different lengths;

d) determining which of said marker shapes were expanded sufficiently to form a valid replacement via to produce a first set of potential replacement vias;

e) eliminating marker shapes that could not be expanded sufficiently to form

a valid replacement via;

f) repeating steps b-e in a second direction perpendicular to said first direction to produce a second set of potential replacement vias; and

g) replacing said stacked vias with said first set of potential replacement vias and said second set of potential replacement vias by removing said stacked vias from said integrated circuit design and adding said first set of potential replacement vias and said second set of potential replacement vias to said integrated circuit design.

16. (Original)The method in claim 15, wherein said locating of said stacked vias and said drawing of said marker shapes is performed using a shapes-processing program.

17. (Original)The method in claim 15, wherein said expanding of said marker shapes is performed using a minimum perturbation layout-migration tool based on augmented ground rules.

18. (Currently Amended) The method in claim 15 ~~10~~, wherein said augmented ground rules direct said layout-migration tool how to modify said marker shapes to reveal when space is available to continue said expanding of said marker shapes.

19. (Original)The method in claim 15, wherein said determining which of said marker shapes were expanded sufficiently is performed using a shapes-processing program.

20. (Original)The method in claim 15, wherein said integrated circuit design complies with design ground rules prior to step a.

21. (Original)A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method for optimizing placement of redundant vias within an integrated circuit design, said method comprising:

a) locating target vias;

b) drawing marker shapes adjacent to said target vias in a first direction;

c) using an optimizer to simultaneously expand all of said marker shapes either in said first direction, wherein during said expanding, different marker shapes will be expanded to different lengths;

d) determining which of said marker shapes were expanded sufficiently to form a valid redundant via to produce a first set of potential redundant vias;

e) eliminating marker shapes that could not be expanded sufficiently to form a valid redundant via; and

f) repeating steps b-e in a second direction perpendicular to said first direction to produce a second set of potential redundant vias.

22. (Original)The program storage device in claim 21, wherein said locating of said target vias and said drawing of said marker shapes is performed using a shapes-processing program.

23. (Original)The program storage device in claim 21, wherein said expanding of said marker shapes is performed using a minimum perturbation layout-migration tool based on augmented ground rules.

24. (Original)The program storage device in claim 23, wherein said augmented ground rules direct said layout-migration tool how to modify said marker shapes to reveal when space is available to continue said expanding of said marker shapes.

25. (Original)The program storage device in claim 21, wherein said determining which of said marker shapes were expanded sufficiently is performed using a shapes-processing program.

26. (Original)The program storage device in claim 21, wherein said integrated circuit design complies with design ground rules prior to step a.

27. (Original)The program storage device in claim 21, wherein said method further comprises after step f, adding redundant vias to said integrated circuit design according to output produced by said optimizer.

REMARKS

Claims 1-17 and 19-27 are all the claims pending in the application. Claim 18 stands rejected upon informalities, and claims 1-17 and 19-27 are allowed. In addition, the Abstract is objected to.

With respect to the objection to the Abstract, the Abstract has been rewritten on a single page with under 150 words. With respect to the claims, claim 18 has been amended to provide the proper claim dependency.

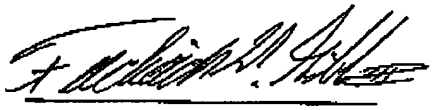
In view of the foregoing, Applicants submit that claims 1-27, all the claims presently pending in the application, are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-09456.

Respectfully submitted,

Dated: 4/6/05



Frederick W. Gibb, III
Reg. No. 37,629

McGinn & Gibb, PLLC
2568-A Riva Road
Suite 304
Annapolis, MD 21401
Customer Number: 29154